Amendments to the Claims:

The listing of claims will replace all prior versions, and listings, of claims in the application:

In the Claims:

1. (Currently Amended) In a software driven emulator comprised of a plurality of ~~modules on~~ printed circuit boards each having a module, each of said modules including a processor chip and at least one SDRAM coupled to the processor chip, a maintenance bus coupled to said SDRAM, and a memory controller coupled to said maintenance bus, a method of executing bulk data transfers to said SDRAM via said maintenance bus, comprising ~~including the steps of~~:

setting a latch in said memory controller to halt data transfer between said SDRAM and said processor chip, said processor chip including a plurality of emulation processors;

transferring data in bursts to said SDRAM from the plurality of emulation processors via said maintenance bus on each clock cycle for a predetermined number of clock cycles in succession;

halting the transfer of data after said predetermined number of clock cycles ~~data transfers~~;

initiating a SDRAM refresh cycle after said halting ~~step~~;

resuming said transferring data in bursts ~~step~~ upon receipt of a done signal after said refresh cycle.

2. (Currently Amended) In a software driven emulator comprised of a plurality of ~~modules on~~ printed circuit boards each having a module, each of said modules including a processor chip and at least one SDRAM coupled to the processor chip, a maintenance bus coupled to said

SDRAM, and a memory controller coupled to said maintenance bus, a method of executing bulk data transfers ~~to~~ from said SDRAM via said maintenance bus, comprising ~~including the steps of~~:

setting a latch in said memory controller to halt data transfer between said SDRAM and said processor chip, said processor chip including a plurality of emulation processors;

transferring data in bursts from said SDRAM to the plurality of emulation processors via said maintenance bus on each clock cycle for a predetermined number of clock cycles in succession;

halting the transfer of data after said predetermined number of clock cycles ~~data transfers~~;

initiating a SDRAM refresh cycle after said halting ~~step~~;

resuming said transferring data in bursts ~~step~~ upon receipt of a done signal after said refresh cycle.

3. (Previously Presented) A method of executing bulk transfers as in claim 1 including establishing a starting address for said bulk transfer in said memory controller and incrementing said starting address by one on each clock cycle.

4. (Previously Presented) A method of executing bulk transfers as in claim 2 including establishing a starting address for said bulk transfer in said memory controller and incrementing said starting address by one on each clock cycle.

5. (Previously Presented) A method of executing bulk transfers as in claim 1 wherein a data word is transferred on each clock cycle.

6. (Previously Presented) A method of executing bulk transfers as in claim 2 wherein a data word is transferred on each clock cycle.